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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,889	10/19/2001	Nobuyuki Sekikawa	492322002200	7319

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MORRISON & FOERSTER
1650 Tysons Blvd.
Suite 300
McLean, VA 22102

[REDACTED] EXAMINER

VU, DAVID

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/981,889	SEKIKAWA ET AL.
	Examiner	Art Unit
	DAVID VU	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 21 April 2003.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) 1-3 and 6-13 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 4,5,14 and 15 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 19 October 2001 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
 If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
 * See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ .
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see paper No. 9, filed on 04/21/03, with respect to the rejection of claims 4-5 and 14-15 have been fully considered and are persuasive. Therefore, the final rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Omura et al. (US 5,883,402) and Yoshida et al. (6,229,180).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 4-5 and 14-15 are rejected under 35 U. S. C. 102(b) as being anticipated by Omura et al.(US 5,883,402)

In regards to claims 4 and 14, Omura et al, in related text (Col. 15, Line 11-Col. 16, Line 6 or Col. 21, lines 52-63; Col. 22, lines 13-27) and figure (Figures. 19-21 and 41, 43-44) disclose a semiconductor device comprising: a resistance layer 29 of a second conductivity type formed on a semiconductor substrate 21/23 of a first conductivity type, one end of resistance layer 29 being adapted to have a first voltage applied thereto, another end of resistance layer being adapted to have a second voltage applied thereto; an oxide film 26 formed on the resistance layer; a resistance bias electrode layer comprising a silicon layer 27 formed on the oxide film 26; and a pair of electrode pad layers of the second conductive type 24 formed at both ends of the resistance layer of the second conductivity type. The intended use limitation beginning "wherein the first and second voltages are applied to the corresponding electrode pad layers to provide the resistance layer with an electric current, and the device is configured so that voltage dependence of a resistance of the resistance layer is reduced by adjusting the first and second voltages applied to the resistance bias electrode layer." does not structurally distinguish the claimed invention over Omura et al.

In regards to claim 5, the intended use limitation beginning "wherein the ratio of the voltage....." does not structurally distinguish the claimed invention over Omura et al.

In regards to claim 14, it would have been obvious to one of ordinary skill in the art at the time the invention was made to consider the resistance bias electrode is formed as two sequentially silicon layers 27 (Figs. 19-21) {or two sequentially silicon layers 58 (Fig. 41)}

composed of the same material since separating what was once one layer, into many layers, involves only routine skill in the art.

In regards to claim 15, the intended use limitation beginning "wherein the voltage applied to the silicon layer...." does not structurally distinguish the claimed invention over Omura et al.

3. Claims 4-5 and 14-15 are rejected under 35 U. S. C. 102(e) as being anticipated by Yoshida et al., (US 6,229,180).

In regards to claims 4 and 14, Yoshida et al., in related text (Col. 8, Line 45-Col. 9, Line 2) and figure (Figure.4) disclose a semiconductor device comprising: a resistance layer of a second conductivity type 64 formed on a semiconductor substrate of a first conductivity type, one end of resistance layer 64 being adapted to have a first voltage applied thereto, another end of resistance layer 64 being adapted to have a second voltage applied thereto; an oxide film formed on the resistance layer 64; a resistance bias electrode layer comprising a silicon layer 68 formed on the oxide film; and a pair of electrode pad layers of the second conductive type 66/63 formed at both ends of the resistance layer of the second conductivity type. The intended use limitation beginning "wherein the first and second voltages are applied to the corresponding electrode pad layers to provide the resistance layer with an electric current, and the device is configured so that voltage dependence of a resistance of the resistance layer is reduced by adjusting the first and second voltages applied to the resistance bias electrode layer." does not structurally distinguish the claimed invention over Yoshida et al.

In regards to claim 5, the intended use limitation beginning "wherein the ratio of the voltage...." does not structurally distinguish the claimed invention over Yoshida et al.

In regards to claim 14, it would have been obvious to one of ordinary skill in the art at the time the invention was made to consider the resistance bias electrode is formed as two sequentially silicon layers 68 composed of the same material since separating what was once one layer, into many layers, involves only routine skill in the art.

In regards to claim 15, the intended use limitation beginning "wherein the voltage applied to the silicon layer...." does not structurally distinguish the claimed invention over Yoshida et al.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (703) 305-0391. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms., can be reached on (703) 308-4910.

DV

David Vu.



David Nelms
Supervisory Patent Examiner
Technology Center 2800